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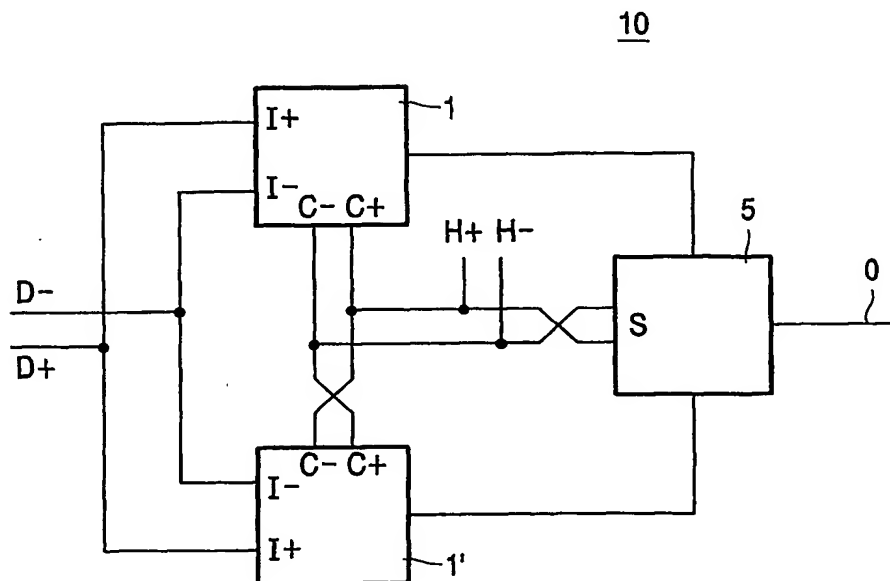
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(54) Title: CIRCUIT FOR USE IN FREQUENCY OR PHASE DETECTOR



(57) Abstract: A tracking data cell (10) comprising: - a pair of track and hold circuits (1, 1') coupled to a first multiplexer (5), - a clock signal (H+, H-) being inputted substantially in anti-phase in the respective track and hold circuits (1, 1') for determining a receipt of a data signal (D+, D-) having a rate, - said track and hold circuits (1, 1') providing an output signal (O) having a substantially half rate.

WO 2004/086409 A1



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